# CS1242

24-bit Sigma-Delta ADC

Rev 1.0

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| | | |
|---|---|---|
| REV 1.0 | LOGO | 2014-10-17 |
| | | |
| | | |
| | | |
| | | |

# 1

CS1242 24bit 22

/

## 1.1

- 24 22
- 50Hz 60Hz 90dB
- INL 0.0015%
- 1 128
-
- ADC
- 0.1V 5V
-
- SPI
- 0.6mW
- 4

## 1.2

-
-
- /
-
-
-

## 1.3

CS1242 24 Sigma-Delta 22

2.7V~5.5V

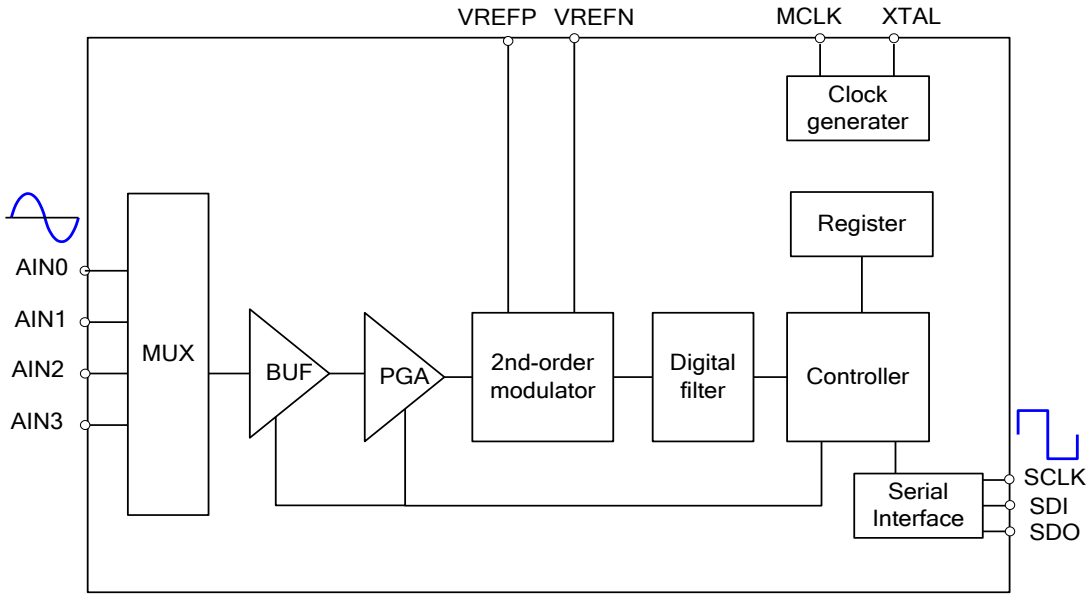
CS1242 Buffer

ADC CS1242 1 128

128 CS1242 18bit Sigma-Delta

FIR 50Hz 60Hz

CS1242 SPI




1 CS1242

# 2

## 2.1

1 CS1242

| | | | | | |
|---|---|---|---|---|---|
| | AVDD | -0.3 | 6 | V | AVDD to AGND |
| | DVDD | -0.3 | 6 | V | DVDD to DGND |
| | DVGND | -0.3 | 0.3 | V | DGND to AGND |
| | | | 100 | mA | Input Current momentary |
| | | | 10 | mA | Input Current continuous |
| | | -0.3 | DVDD+0.3 | V | Digital Output Voltage to DGND |
| | | -0.3 | DVDD+0.3 | V | |
| | | | 150 | $^{o}$C | Max. Junction Temperature |
| | | -40 | 85 | $^{o}$C | Operating Temperature |
| | | -60 | 150 | $^{o}$C | Storage Temperature |
| | | | 300 | $^{o}$C | Lead Temperature (Soldering, 10s) |

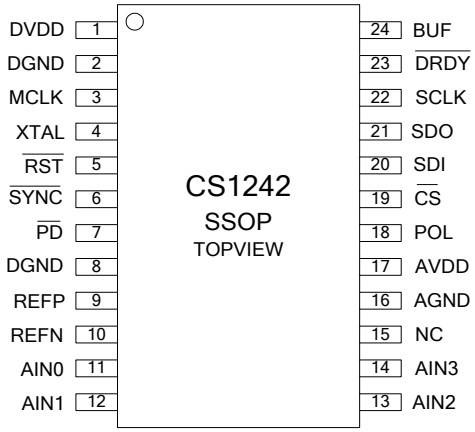
## 2.2

2 CS1242

| | | | | | |
|---|---|---|---|---|---|
| VIH | 0.8 DVDD | | DVDD | V | |
| VIL | DGND | | 0.2 DVDD | V | |
| VOH | DVDD-0.4 | | DVDD+0.4 | V | Ioh=1mA |
| VOL | DGND | | DGND+0.4 | V | IoL=1mA |
| IIH | | | 10 | uA | VI=DVDD |
| IIL | -10 | | | uA | VI=DGND |
| fosc | 1 | | 5 | MHz | |
| tosc | 200 | | 1000 | ns | |

1 CS1242 CMOS

## 2.3




2 CS1242

3 CS1242

| | | | |
|---|---|---|---|
| 1 | DVDD | 2.7~5.25V | |
| 2 | DGND | | |
| 3 | MCLK | 1 10MHz | |
| 4 | XTAL | 2 | |
| 5 | $\overline{\text{RST}}$ | | |
| 6 | $\overline{\text{SYNC}}$ | | |
| 7 | $\overline{\text{PD}}$ | | |
| 8 | DGND | | |
| 9 | REFP | | |
| 10 | REFN | | |
| 11 | AIN0 | 0 | |
| 12 | AIN1 | 1 | |
| 13 | AIN2 | 2 | |
| 14 | AIN3 | 3 | |
| 15 | NC | | |
| 16 | AGND | | |
| 17 | AVDD | 2.7V~5.25V | |
| 18 | POL | | |
| 19 | $\overline{\text{CS}}$ | | |
| 20 | SDI | | |
| 21 | SDO | | |
| 22 | SCLK | Schmitt | |
| 23 | $\overline{\text{DRDY}}$ | | |
| 24 | BUF | | |

## 2.4

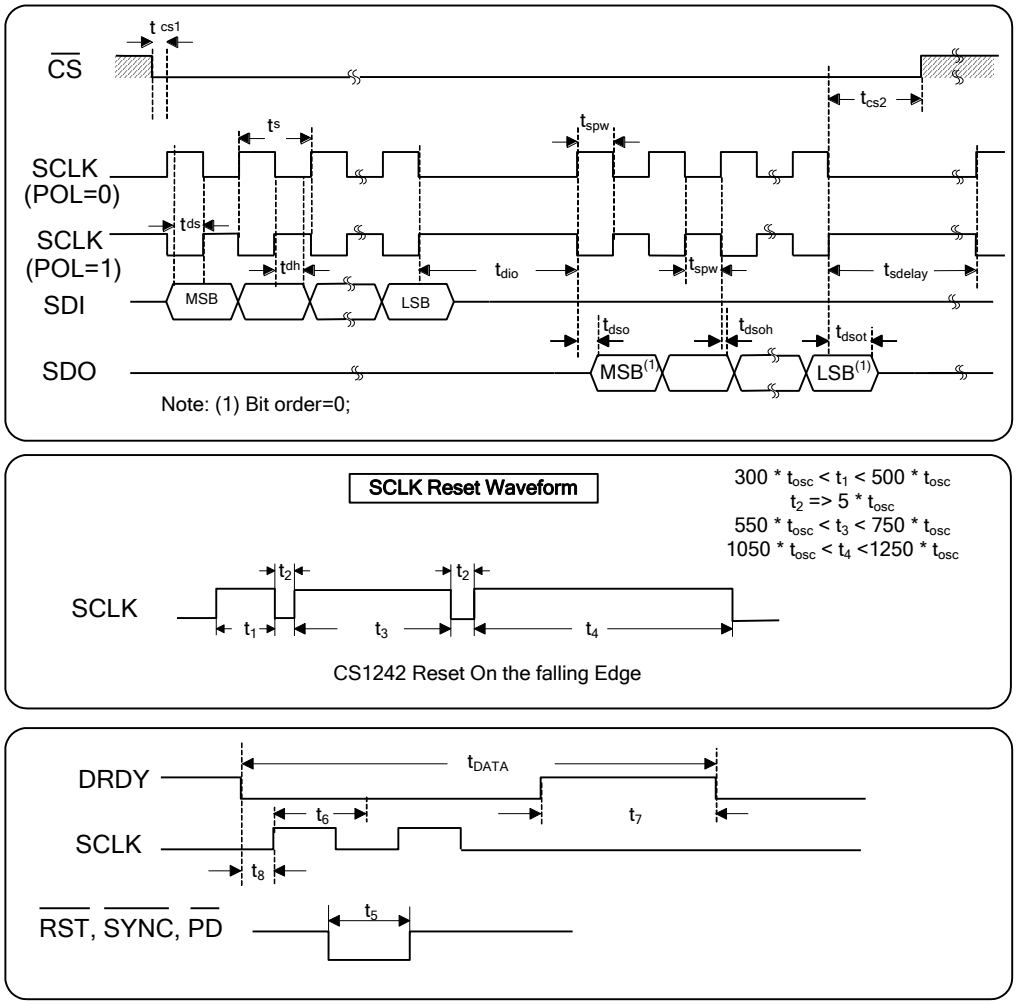
4 AVDD=5V CS1242

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Buffer | AGND-0.1 | | AVDD+0.1 | V |
| | | Buffer | AGND+0.4 | | AVDD-1.5 | V |
| | (AIN+) - (AIN-) | RAN=0 | | | VREF/PGA | V |
| | | RAN=1 | | | VREF/(2 PGA) | V |
| | | Buffer | | 5/PGA | | MΩ |
| | | Buffer | | 5 | | GΩ |
| | -3dB | $f_{DATA}$ = 3.75Hz | | 1.65 | | Hz |
| | | $f_{DATA}$ = 7.50Hz | | 3.44 | | Hz |
| | | $f_{DATA}$ = 15.0Hz | | 3.7 | | Hz |
| | PGA | | 1 | | 128 | |
| | | | | 9 | | pF |
| | | T = 25 | | 5 | | pA |
| | | | | 2 | | 2uA |
| | | | | 24 | | Bits |
| | | | | | 0.0015 | % of FS |
| | | | | 8 | | ppm of FS |
| | | | | 0.02 | | ppm of FS/ |
| | | | | 0.005 | | % |
| | | | | 0.5 | | ppm/ |
| | | | 100 | | | dB |
| | | $f_{CM}$ = 60Hz, $f_{DATA}$ = 15Hz | | 130 | | dB |
| | | $f_{CM}$ = 50Hz, $f_{DATA}$ = 15Hz | | 120 | | dB |
| | | $f_{CM}$ = 60Hz, $f_{DATA}$ = 15Hz | | 100 | | dB |
| | | $F_{CM}$ = 50Hz, $f_{DATA}$ = 15Hz | | 100 | | dB |
| | | | 80 | 95 | | dB |
| | VREF REFP REFN | RAN = 0 | 0.1 | 2.5 | 2.6 | V |
| | | RAN = 1 | 0 | 2.5 | AVDD | V |
| | REFP REFN | RAN = 0 | 0 | | AVDD | V |
| | | RAN = 1 | 0.1 | | AVDD | V |
| | | | | 120 | | dB |
| | | $f_{VREFCM}$ = 60Hz | | 120 | | dB |
| | | | | 1.3 | | uA |
| | | AVDD | 4.75 | | 5.25 | V |
| | | $\overline{PD}$ = 0 | | 1 | | nA |
| | | PGA = 1 Buffer | | 120 | | uA |
| | | PGA = 1 Buffer | | 160 | | uA |
| | | PGA = 128 Buffer | | 400 | | uA |
| | | PGA = 128 Buffer | | 760 | | uA |
| | (DVDD = 5V) | | | 2 | | mA |
| | | | | 2.2 | | mA |
| | | $\overline{PD}$ = 0 | | 0.5 | | nA |

5 AVDD=3V CS1242

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Buffer | AGND-0.1 | | AVDD+0.1 | V |
| | | Buffer | AGND+0.3 | | AVDD-1.5 | V |
| | | RAN=0 | | | VREF/PGA | V |
| | (AIN+) - (AIN-) | RAN=1 | | | VREF/(2 PGA) | V |
| | | Buffer | | 5/PGA | | MΩ |
| | | Buffer | | 5 | | GΩ |
| | | $f_{DATA}$ = 3.75Hz | | 1.65 | | Hz |
| | -3dB | $f_{DATA}$ = 7.50Hz | | 3.44 | | Hz |
| | | $f_{DATA}$ = 15.0Hz | | 14.6 | | Hz |
| | PGA | | 1 | | 128 | |
| | | | | 9 | | pF |
| | | T = 25 | | 5 | | pA |
| | | | | 2 | | 2uA |
| | | | | 24 | | Bits |
| | | | | | 0.0015 | % of FS |
| | | | | 15 | | ppm of FS |
| | | | | 0.04 | | ppm of FS/ |
| | | | | 0.01 | | % |
| | | | | 1.0 | | ppm/ |
| | | | 100 | | | dB |
| | | $f_{CM}$ = 60Hz, $f_{DATA}$ = 15Hz | | 130 | | dB |
| | | $f_{CM}$ = 50Hz, $f_{DATA}$ = 15Hz | | 120 | | dB |
| | | $f_{CM}$ = 60Hz, $f_{DATA}$ = 15Hz | | 100 | | dB |
| | | $f_{SIG}$ = 50Hz, $f_{DATA}$ = 15Hz | | 100 | | dB |
| | | | 75 | 90 | | dB |
| | VREF REFP REFN | RAN = 0 | 0.1 | 1.25 | 1.30 | V |
| | | RAN = 1 | 0 | 2.5 | 2.6 | V |
| | REFP REFN | RAN = 0 | 0 | | AVDD | V |
| | | RAN = 1 | 0.1 | | AVDD | V |
| | | | | 120 | | dB |
| | | $f_{VREFCM}$ = 60Hz | | 120 | | dB |
| | | | | 0.65 | | uA |
| | | AVDD | 2.7 | | 3.3 | V |
| | | $\overline{PD}$ = 0 | | 1 | | nA |
| | | PGA = 1 Buffer | | 107 | | uA |
| | | PGA = 1 Buffer | | 118 | | uA |
| | | PGA = 128 Buffer | | 360 | | uA |
| | | PGA = 128 Buffer | | 500 | | uA |
| | | | | 2 | | mA |
| | (DVDD = 3V) | | | 2.2 | | mA |
| | | $\overline{PD}$ = 0 | | 0.5 | | nA |

## 2.5


t cs1
CS
tcs2
ts
tspw
SCLK (POL=0)
SCLK (POL=1)
tds
tdh
tdio
tspw
tsdelay
SDI
MSB
LSB
tdso
tdsoh
tdsot
SDO
MSB(1)
LSB(1)
Note: (1) Bit order=0;
SCLK Reset Waveform
300 * tosc < t1 < 500 * tosc
t2 => 5 * tosc
550 * tosc < t3 < 750 * tosc
1050 * tosc < t4 <1250 * tosc
SCLK
t1
t2
t3
t4
CS1242 Reset On the falling Edge
DRDY
tDATA
t6
t7
SCLK
t8
RST, SYNC, PD
t5

3 CS1242

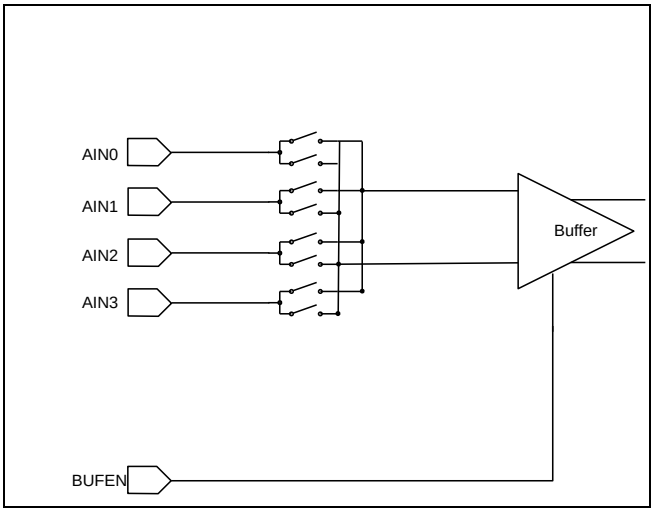
6 CS1242

| | | | | | |
|---|---|---|---|---|---|
| $t_s$ | SCLK | | 4 | | tosc |
| $t_{spw}$ | SCLK | | 200 | | ns |
| $t_{cs1}$ | CS SCLK | | 0 | | ns |
| $t_{ds}$ | SDI SCLK | | 50 | | ns |
| $t_{dsh}$ | SDI | | 50 | | ns |
| $t_{dio}$ | SDI SCLK SDO SCLK RDATA, RDATAC, RREG, WREG | | 50 | | tosc |
| $t_{dso}$ | SDO SCLK | | | 50 | ns |
| $t_{dsoh}$ | SDO | | 0 | | |
| $t_{dsot}$ | SDO SCLK | | 6 | 10 | tosc |
| $t_{cs2}$ | CS SCLK | | 0 | | ns |
| $t_{sdelay}$ | SCLK | RREG, WREG, SYNC, SLEEP, RDATA, RDATAC, STOPC | 4 | | tosc |
| | | GCALSELF, SELFOCA, OCALSYS, GCALSYS | 8 | | DRDY |
| | SCLK | CALSELF | 15 | | DRDY |
| | | RESET SCLK $\overline{RST}$ RESET | 16 | | tosc |
| $t_5$ | | | 4 | | tosc |
| $t_6$ | | | | 5000 | tosc |
| $t_7$ | DOR DOR | | 4 | | tosc |
| $t_8$ | DRDY SCLK | RDATAC | 10 | | tosc |
| | | | 0 | | tosc |

# 3

## 3.1 Input Multiplexer

CS1242 4




4

CS1242 2 3 AIN1

CS1242

DRDY MUX

## 3.2 Buffer

(Buffer) 5MΩ/PGA

5GΩ

BUF ACR BUF ACR

BUF

PGA PGA 1

50uA PGA 128 150uA

AGND+0.3V

AVDD-1.5V

## 3.3 PGA

1 2 4 8 16 32 64 128 PGA

PGA 1 5V 1uV

PGA 128 39mV 75nV

## 3.4 Modulator

CS1242 2 Σ Δ SPEED ACR bit 5

7

| MHz | SPEED | ADC KHz | Hz DR 00 | Hz DR 01 | Hz DR 10 | Hz |
|---|---|---|---|---|---|---|
| 2.4576 | 0 | 19.200 | 15 | 7.5 | 3.75 | 50/60 |
| | 1 | 9.600 | 7.5 | 3.75 | 1.875 | 25/30 |
| 4.9152 | 0 | 38.400 | 30 | 15 | 7.5 | 100/120 |
| | 1 | 19.200 | 15 | 7.5 | 3.75 | 50/60 |

## 3.5 Calibration

OCAL GCAL DRDY AD PGA DRDY DRDY

### 3.5.1 Self Calibration

CS1242 CALSELF GCALSELF OCALSELF CALSELF Offset Calibration Gain Calibration GCALSELF OCALSELF 8 TDATA AD TDATA SEFLCAL 15 TDATA CS1242 CS1242 PGA 1 CS1242 PGA PGA AVDD 1.5V

### 3.5.2 System Calibration

OCALSYS GCALSYS OCALSYS GCALSYS 8 TDADA

OCALSYS 0 CS1242

OCC CS1242

SYSGCAL CS1242

GCC CS1242

## 3.6 External Voltage Reference

CS1242 ACR REFP REFN

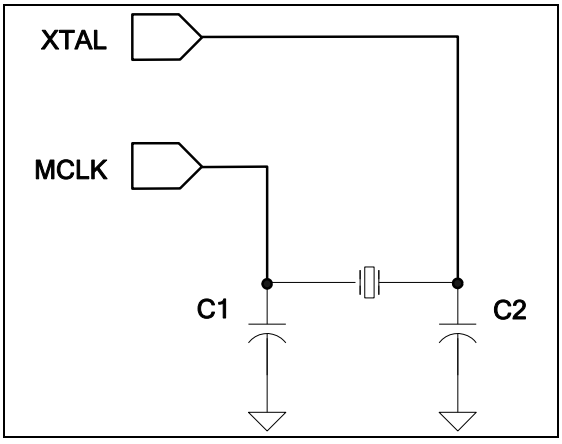
8 RAN

| RAN ACR.2 | V | V | |
|---|---|---|---|
| 0 | 5 | <=2.5 | |
| 1 | 5 | <=5 | |
| 0 | 3.0 | <=1.25 | |
| 1 | 3.0 | <=2.5 | |

## 3.7 Clock Unit

CS1242 MCLK XTAL

MCLK XTAL 10 20pF




5

## 3.8 (FIR)

CS1242 FIR FIR

2.4576M CS1242 15Hz 7.5Hz 3.75Hz

FIR 50Hz 60Hz

3.6864M

( 3.6864MHz/2.4576MHz ) ×15Hz = 22.5Hz

( 3.6864MHz/2.4576MHz ) ×( 50Hz 60Hz ) ( 75Hz 90Hz )

## 3.9 ( SPI )

CS1242 SPI CS1242
SPI CS SCLK SDI SDO POL
POL

### 3.9.1 ( CS )

CS1242 CS CS
CS SPI CS
CS SPI

### 3.9.2 ( SCLK )

SCLK SDI SDO SCLK
3 DRDY SCLK SCLK
SPI SCLK
**RESET**

### 3.9.3 ( POL )

POL SCLK POL SCLK
SCLK POL SCLK
SCLK

### 3.9.4 ( SDI ) ( SDO )

SDI SDO SDO
SDI SDO
CS1242 RDATAC RDATAC STOPC RESET
RDATAC
CS1242 STOPC RESET RDATAC
SDO STOPC RESET SDI STOPC
RESET RDATAC

### 3.9.5 ( DRDY )

DRDY DOR
DRDY DOR DRDY
DOR DRDY DOR
DOR DOR

DRDY ACR bit 7

### 3.10 SYNC

CS1242 SYNC SYNC SYNC

SYNC SYNC

SYNC RESET

SYNC SYNC SCLK

RESET SCLK SYNC

SCLK

### 3.11

CS1242 $\overline{\text{RST}}$ RESET SCLK

( SCLK RESET CS1242 )

# 4 CS1242

CS1242

## 4.1

9

| (H) | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | SETUP | ID3 | ID2 | ID1 | ID0 | | PGA2 | PGA1 | PGA0 |
| 01 | MUX | PS3 | PS2 | PS1 | PS0 | NS3 | NS2 | NS1 | NS0 |
| 02 | ACR | $\overline{\text{DRDY}}$ | U/$\overline{\text{B}}$ | SPEED | BUF | BITOR | RAN | DR1 | DR0 |
| 03 | ODAC | | CHSEL | ISET1 | ISET0 | | | | |
| 04 | | | | | | | | | |
| 05 | | | | | | | | | |
| 06 | | | | | | | | | |
| 07 | OCC0 | OCC07 | OCC06 | OCC05 | OCC04 | OCC03 | OCC02 | OCC01 | OCC00 |
| 08 | OCC1 | OCC17 | OCC16 | OCC15 | OCC14 | OCC13 | OCC12 | OCC11 | OCC10 |
| 09 | OCC2 | OCC27 | OCC26 | OCC25 | OCC24 | OCC23 | OCC22 | OCC21 | OCC20 |
| 0A | GCC0 | GCC07 | GCC06 | GCC05 | GCC04 | GCC03 | GCC02 | GCC01 | GCC00 |
| 0B | GCC1 | GCC15 | GCC14 | GCC13 | GCC12 | GCC11 | GCC10 | GCC09 | GCC08 |
| 0C | GCC2 | GCC23 | GCC22 | GCC21 | GCC20 | GCC19 | GCC18 | GCC17 | GCC16 |
| 0D | DOR2 | DOR23 | DOR22 | DOR21 | DOR20 | DOR19 | DOR18 | DOR17 | DOR16 |
| 0E | DOR1 | DOR15 | DOR14 | DOR13 | DOR12 | DOR11 | DOR10 | DOR09 | DOR08 |
| 0F | DOR0 | DOR07 | DOR06 | DOR05 | DOR04 | DOR03 | DOR02 | DOR01 | DOR00 |

## 4.2

**SETUP** 00H xxxx0000 PGA SETUP REGISTER

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| ID3 | ID2 | ID1 | ID0 | | PGA2 | PGA1 | PGA0 |

SETUP. 7 4 : ID
SETUP.3 :
SETU.2 0 PGA2/PGA1/PGA0 (Programmable Gain Amplifier Gain Selection)
000 1
001 2
010 4
011 8
100 16
101 32
110 64
111 128

**MUX** 01H 01H Multiplexer Control Register

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| PS3 | PS2 | PS1 | PS0 | NS3 | NS2 | NS1 | NS0 |

**MUX**. 7 4 : PS3 0 Positive Channel Selection
0000 ADIN0
0001 ADIN1
0010 ADIN2
0011 ADIN3
Reserved
**MUX**. 3 0 : NS3 0 Negative Channel Selection
0000 ADIN0
0001 ADIN1
0010 ADIN2
0011 ADIN3
Reserved

**ACR** 02H, 00H Analog Control Register

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| $\overline{DRDY}$ | U/$\overline{B}$ | SPEED | BUF | BITOR | RAN | DR1 | DR0 |

**ACR**.7 : $\overline{DRDY}$ Data Ready $\overline{DRDY}$

**ACR**.6 : U/$\overline{B}$ Data Format

0

*FSR 0x7FFFFFH ZERO 0x00000H FSR 0x800000H;*

1

*FSR 0xFFFFFFH ZERO 0x00000H FSR 0x000000H;*

**ACR**.5 : SPEED Modulator Clock Speed

0 fosc/128

1 fosc/256

**ACR**.4 : BUF Buffer Enable

0

1

**ACR**.3 : BITOR bit

0 =

1 =

**ACR**.2 : RAN Select

0 Full Scale / $V_{REF}$

1 Full Scale / $V_{REF}$/2

**ACR**.1-0 : DR1/DR0 Data Rate

00 15Hz

01 7.5Hz

10 3.75Hz;

11= Reserved

**ODAC** 03H, 00H Offset DAC

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | CHSEL | ISET1 | ISET0 | | | | |

ISET1-0

00 10uA

01 10 25

11 50

CS1242

CHSEL

0 1/2 PGA=1~128

1 PGA 2~128

CHSEL 0

CHSEL 1

**OCC0** 07H, 00H Offset Calibration Coefficient

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| OCC07 | OCC06 | OCC05 | OCC04 | OCC03 | OCC02 | OCC01 | OCC00 |
| OCC0 OCC1 OCC2 OCC23~0 24 OCC23 MSB OCC00 LSB | | | | | | | |

**OCC1** 08H, 00H Offset Calibration Coefficient

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| OCC15 | OCC14 | OCC13 | OCC12 | OCC11 | OCC10 | OCC09 | OCC08 |
| OCC0 OCC1 OCC2 OCC23~0 24 OCC23 MSB OCC00 LSB | | | | | | | |

**OCC2** 09H, 00H Offset Calibration Coefficient

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| OCC23 | OCC22 | OCC21 | OCC20 | OCC19 | OCC18 | OCC17 | OCC16 |
| OCC0 OCC1 OCC2 OCC23~0 24 OCC23 MSB OCC00 LSB | | | | | | | |

**GCC0** 0AH, 59H Gain Calibration Coefficient

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| GCC07 | GCC06 | GCC05 | GCC04 | GCC03 | GCC02 | GCC01 | GCC00 |
| GCC0 GCC1 GCC2 GCC23~0 24 GCC23 MSB GCC00 LSB | | | | | | | |

**GCC1** 0BH, 55H Gain Calibration Coefficient

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| GCC15 | GCC14 | GCC13 | GCC12 | GCC11 | GCC10 | GCC09 | GCC08 |
| GCC0 GCC1 GCC2 GCC23~0 24 GCC23 MSB GCC00 LSB | | | | | | | |

**GCC2** 0CH, 55H Gain Calibration Coefficient

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| GCC23 | GCC22 | GCC21 | GCC20 | GCC19 | GCC18 | GCC17 | GCC16 |
| GCC0 GCC1 GCC2 GCC23~0 24 GCC23 MSB GCC00 LSB | | | | | | | |

**DOR2** 0DH 00H Data Output Register

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DOR 23 | DOR22 | DOR 21 | DOR 20 | DOR 19 | DOR 18 | DOR 17 | DOR 16 |
| DOR 0 DOR 1 DOR 2 DOR23~0 24 DOR23 MSB DOR00 LSB | | | | | | | |

**DOR1** 0EH 00H Data Output Register

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DOR15 | DOR14 | DOR13 | DOR12 | DOR11 | DOR10 | DOR09 | DOR08 |
| DOR 0 DOR 1 DOR 2 DOR23~0 24 DOR23 MSB DOR00 LSB | | | | | | | |

**DOR0** 0FH, 00H Data Output Register

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| DOR07 | DOR06 | DOR05 | DOR04 | DOR03 | DOR02 | DOR01 | DOR00 |
| DOR 0 DOR 1 DOR 2 DOR23~0 24 DOR23 MSB DOR00 LSB | | | | | | | |

# 5 CS1242

CS1242

RESET WREG

n = 0 127

r = ( 0 15 )

x =

## 5.1

10 CS1242

| | | | |
|---|---|---|---|
| RDATA | DOR | 0000 0001 ( $01_H$ ) | -- |
| RDATAC | DOR | 0000 0011 ( $03_H$ ) | -- |
| STOPC | DOR | 0000 1111 ( $0F_H$ ) | -- |
| RREG | rrrr | 0001 r r r r ( $1X_H$ ) | xxxx_nnnn |
| WREG | rrrr | 0101 r r r r ( $5X_H$ ) | xxxx_nnnn |
| CALSELF | | 1111 0000 ( $F0_H$ ) | |
| OCALSELF | | 1111 0001 ( $F1_H$ ) | |
| GCALSELF | | 1111 0010 ( $F2_H$ ) | |
| OCALSYS | | 1111 0011 ( $F3_H$ ) | |
| GCALSYS | | 1111 0100 ( $F4_H$ ) | |
| SYNC | DRDY | 1111 1100 ( $FC_H$ ) | |
| RESET | | 1111 1110 ( $FE_H$ ) | |
| | | ACR BITORDER | |

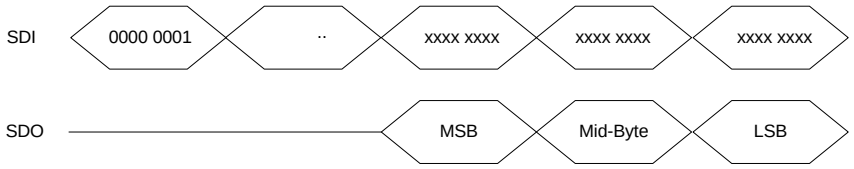
## 5.2

### RDATA

DOR AD 24bit

1

0000 0001




### RDATAC

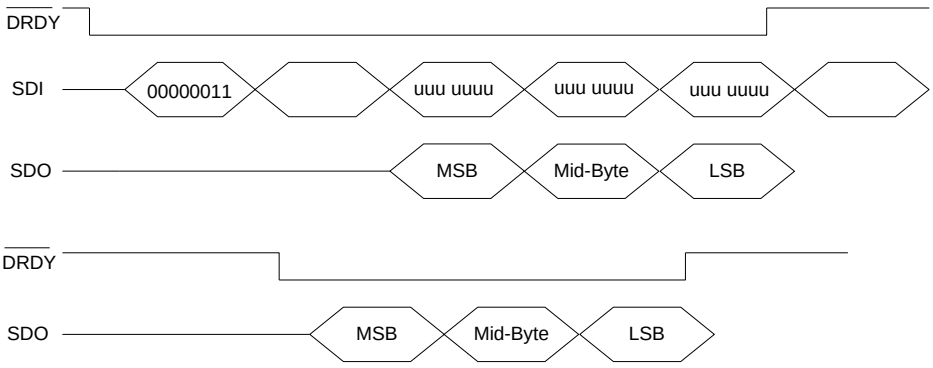
RDATAC DRDY DOR AD

DRDY RDATA STOPC

RESET DRDY 10 $f_{OSC}$

1

0000 0011

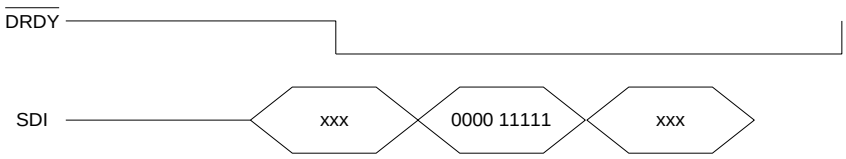



### STOPC

DRDY

1

0000 1111




## RREG

16

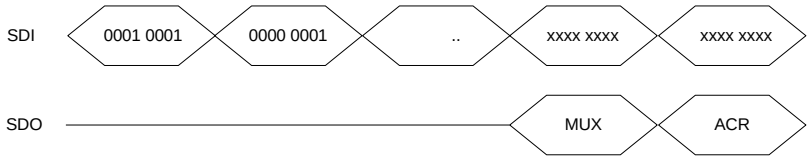
1

r, n

2

0001 rrrr xxxx nnnn

$01_H$ ( MUX )




## WREG

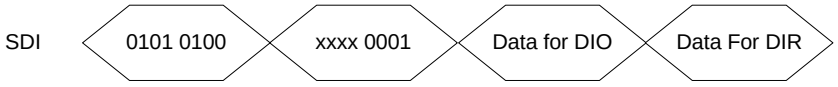
1

r, n

2

0101 rrrr xxxx nnnn

$04_H$ ( DIO )

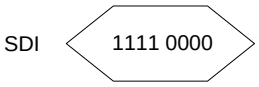



## CALSELF

OCC GCC

1

1111 0000

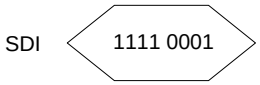


**OCALSELF**

OCC

1

1111 0001

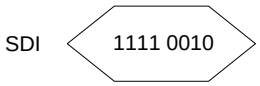



**GCALSELF**

GCC

1

1111 0010




**OCALSYS**

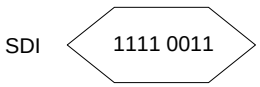
0 CS1242

OCC OCC

0 OCC

1

1111 0011



**GCALSYS**

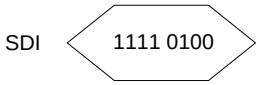
CS1242

GCC OCC

GCC

1

1111 0100

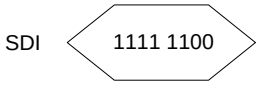



**SYNC DRDY**

CS1242

1

1111 1100

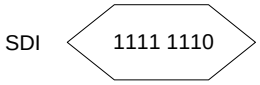



**RESET**

RDATAC

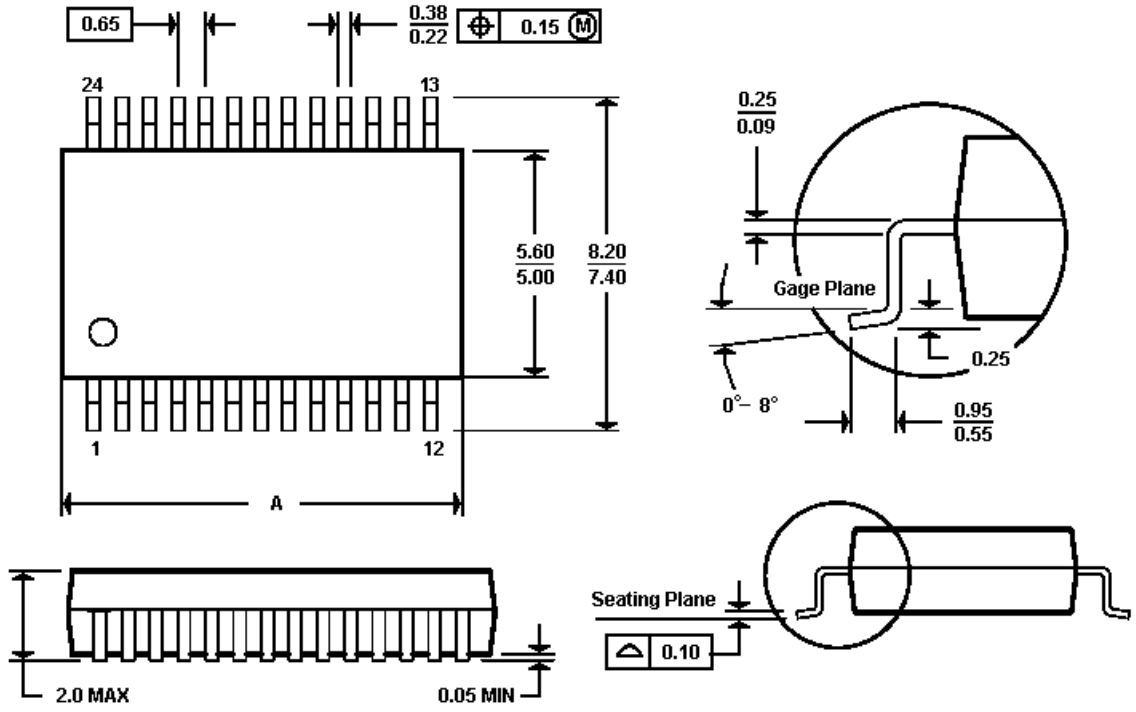
1

1111 1110



# 6

CS1242 SSOP-24




NOTES :

A. All linear dimensions are in millimeters
B. This drawing is subject to change without notice
C. Body demensions do not include mold flash or protrusion nont to exceed 0.15
D. Falls within JEDEC MO-150

| DIM \ PINS | 24 | 28 |
|---|---|---|
| A MAX | 9.50 | 10.50 |
| A MIN | 7.90 | 9.90 |

6 SSOP-24