芯海科技
CHIPSEA

CS1237

24-bit Sigma-Delta ADC

Rev 1.1

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REV 1.0		2014-3-26
REV 1.1	1. 2. 3. P-P 4.	2014-10-17

1

CS1237

CS1237 PGA 1 2 64 128 128

CS1237 ADC 10Hz 40Hz 640Hz 1.28kHz 10Hz

MCU 2 SPI SCLK $\overline{DRDY}$ / $DOUT$ CS1237 PGA

1.1

-
-
- Power down
- 2 SPI 1.1MHz

ADC

- 24
- PGA 1 2 64 128
- 1 24 PGA=128 ENOB 20 (5V)\19.5 (3.3V)
- P-P PGA=128 10Hz 180nV
- INL 0.0015%
- 10Hz 40Hz 640Hz 1.28kHz
-

1.2

-
-
- /
-
-
-

1.3

CS1237 Sigma-Delta Sigma-Delta ADC ADC sigma delta

PGA 1 2 64 128 PGA=128

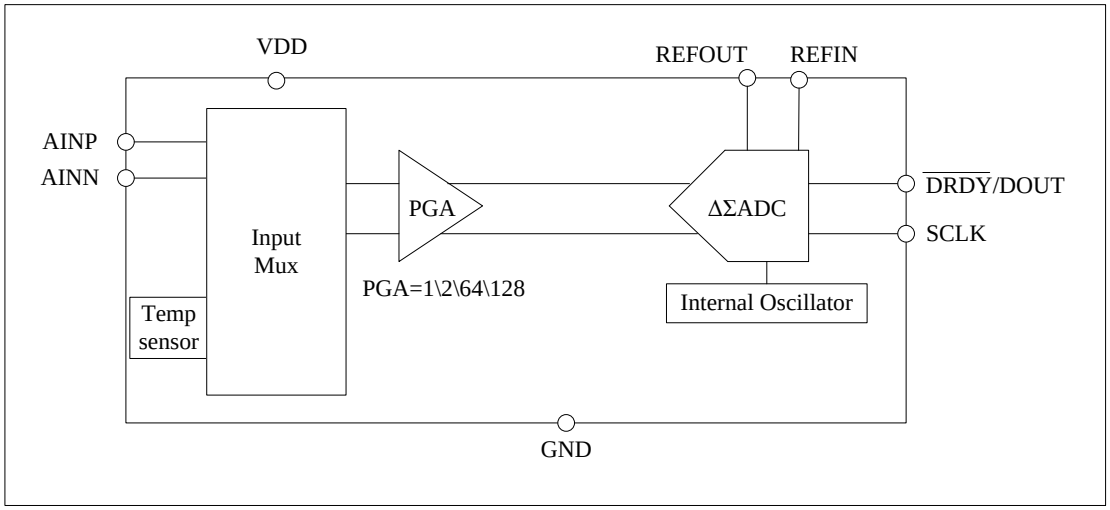
20 (5V)

CS1237 RC

CS1237 $\overline{DRDY}$ / *DOUT* SCLK

PGA ADC

CS1237 Power down



1 CS1237

1.4

1 CS1237

	VDD	-0.3	6	V
			100	mA
			10	mA
		-0.3	DVDD+0.3	V
		-0.3	DVDD+0.3	V
			150	
		-40	85	
		-60	150	
			240	

1.5 CS1237

2 CS1237

VIH	0.7×DVDD		DVDD+0.1	V	
VIL	DGND		0.3×DVDD	V	
VOH	DVDD-0.4		DVDD	V	Ioh=1mA
VOL	DGND		0.2×DVDD	V	IoL=1mA
IIH			10	μA	VI=DVDD
IIL	-10			μA	VI=DGND
SCLK			1.1	MHz	

1.6 CS1237

-40~85

3 CS1237 VDD = 5V 3.3V

(AINP-AINN)			±0.5VREF/PGA		V
	PGA=1 2	AGND-0.1		AVDD+0.1	V
	PGA=64 128	AGND+0.75		AVDD-0.75	V
	PGA=1 2		190		MΩ
	PGA=64 128		28		MΩ
			24		Bits
AD			10	1280	Hz
		3 ADC 10\40Hz 4 ADC 640\1280Hz			
P-P	PGA=128 10Hz		180		nv
	PGA=128 10Hz		20 5V 19.5 3.3V		Bit
	PGA=128		±15		ppm
	PGA=128		±1.4		μV
	PGA=128		20		nv/
	PGA=128		±0.5		%
	PGA=128		8		ppm/
	REFIN	1.5	VDD	VDD+0.1	V
	REFOUT		VDD		V
			5.2		MHz
			250		ppm/
	TempError		±3		

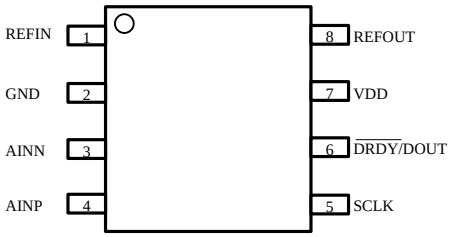
4 CS1237 VDD = 5V

	VDD	4.5	5	5.5	V
	PGA=1 2		1.57		mA
	PGA=64 128		2.34		mA
	Power down		0.1	0.1	μA

5 CS1237 VDD = 3.3V

	VDD	3	3.3	3.6	V
	PGA=1 2		1.26		mA
	PGA=64 128		2.11		mA
	Power down		0.1		μA

1.7



2 CS1237

6 PIN

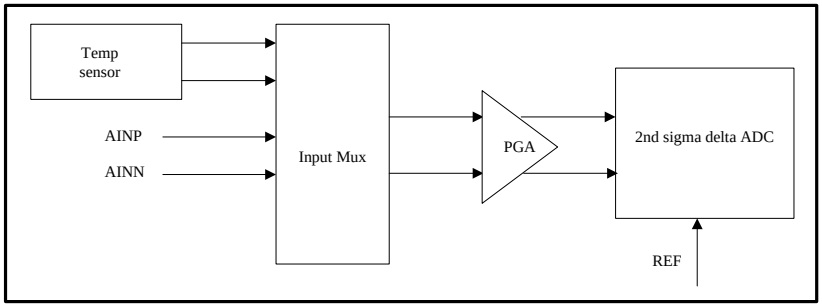
		/	
1	REFIN	AI	
2	GND	P	
3	AINN	AI	
4	AINP	AI	
5	SCLK	DI	SPI
6	$\overline{DRDY}/DOUT$	DI/DO	SPI \
7	VDD	P	
8	REFOUT	AO	

REFOUT VDD

2

2.1

CS1237 1 ADC 1 AINP
AINN (ch_sel[1:0])



3

CS1237 PGA 1 2 64 128 (pga_sel[1:0])

(refo_off)

2.2

ch_sel[1:0]=2’b10 ADC

ADC

ch_sel[1:0]=2’b10 ADC PGA=1

A **Ya**

B **= Yb*(273.15+A)/Ya-273.15**

A **Ya** **A** **Yb** **B**

2.3 PGA

CS1237 PGA

EMI R=450Ω C=18pF 20M

PGA RF1 R1 RF2 64 PGA 64

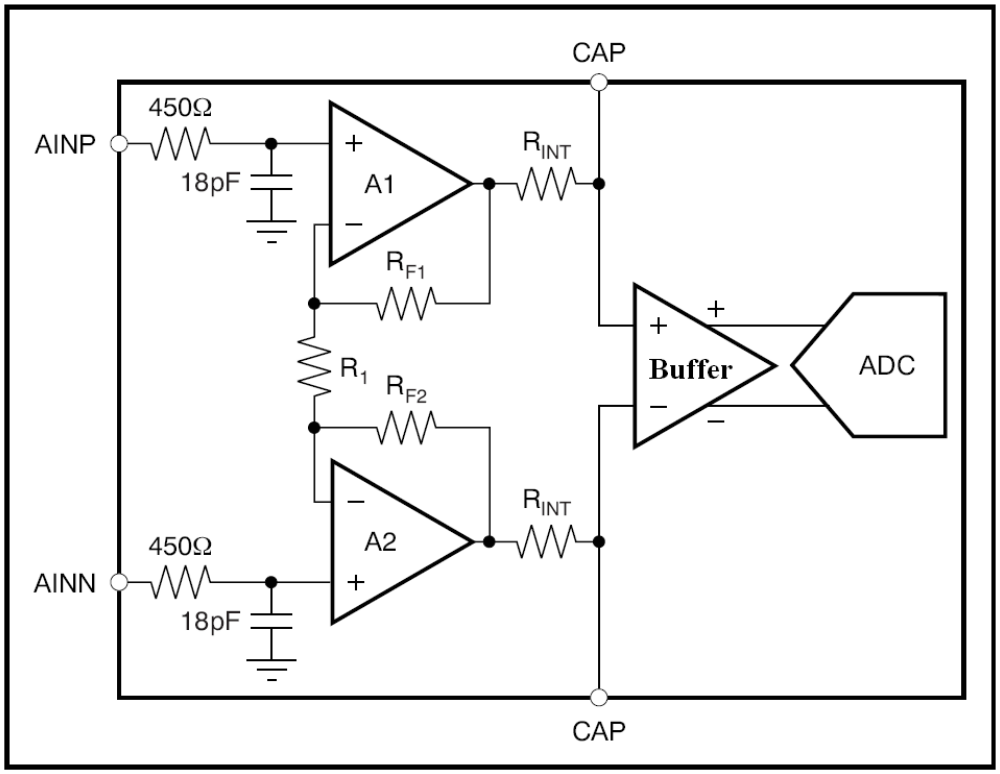
128 PGA pga_sel[1:0] 1 2 64 128 PGA

PGA=1 2 64 PGA PGA

GND+0.75V VDD-0.75V

CAP 45pF 2k RINT

PGA ADC



4 PGA

CS1237 Buffer PGA=1 2 CS1237 Buffer ADC

PGA=64 128

CS1237 Buffer PGA RINT=2K CINT=0.1μF

2.4

CS1237 5.2MHz

2.5 (POR&power down)

SCLK 100μs CS1237 PowerDwon 0.1μA SCLK

Power down PowerDown

2.6 SPI

CS1237 2 SPI SCLK $\overline{DRDY}/DOUT$

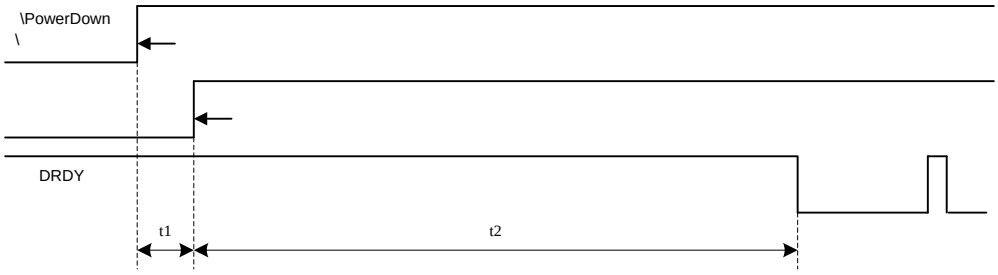
2.6.1

ADC 10Hz 40Hz 3

ADC 640Hz 1280Hz

4

CS1237



5 CS1237 1

6 CS1237 2

	(1)					
t1	\PowerDown \			2		ms
t3	PGA \			0.8		μs
t2	($\overline{DRDY}/DOUT$)	10\40Hz		300\75		ms
		640\1280Hz		6.25\3.125		ms

2.6.2 ADC

CS1237 speed_sel[1:0]

7

SPEED_SEL[1:0]	ADC (Hz)
00	10
01	40
10	640
11	1280

2.6.3

CS1237 24 2 MSB

LSB $(0.5V_{REF}/Gain)/(2^{23}-1)$ 7FFFFFH

800000H

8 (1)

V_{IN} AINP-AINN	
$+0.5V_{REF}/Gain$	7FFFFFH
$(+0.5V_{REF}/Gain)/(2^{23}-1)$	000001H
0	000000H
$(-0.5V_{REF}/Gain)/(2^{23}-1)$	FFFFFFH
$+0.5V_{REF}/Gain$	800000H

1 INL

2.6.4 / ($\overline{DRDY}$ / *DOUT*)

$\overline{DRDY}$ / *DOUT* 4

1 SCLK $\overline{DRDY}$ / *DOUT*

MSB SCLK 1 24

SCLK 24 SCLK $\overline{DRDY}$ / *DOUT*

$\overline{DRDY}$ / *DOUT*

25 26 SCLK

SPI 46 SCLK $\overline{DRDY}$ / *DOUT*

2.6.5 (SCLK)

SCLK

SCLK

50ns

2.6.6

CS1237 $\overline{DRDY}/DOUT$

SCLK 24 SCLK

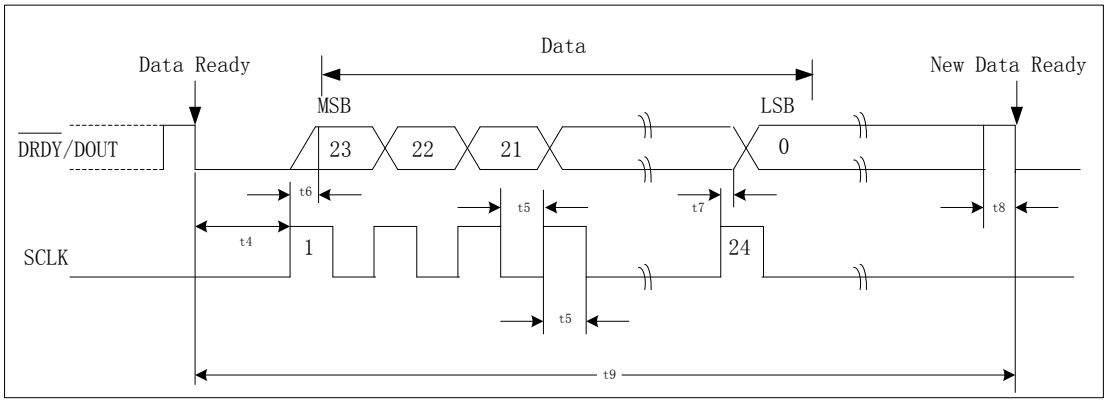
24 SCLK $\overline{DRDY}/DOUT$

25 26 SCLK 25

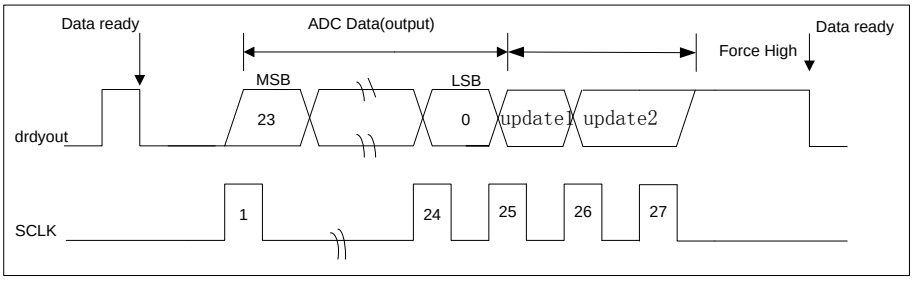
SCLK $\overline{DRDY}/DOUT$ 1 Config 26

SCLK $\overline{DRDY}/DOUT$ 0 27 SCLK

$\overline{DRDY}/DOUT$ $\overline{DRDY}/DOUT$



7 CS1237 1



8 CS1237 2

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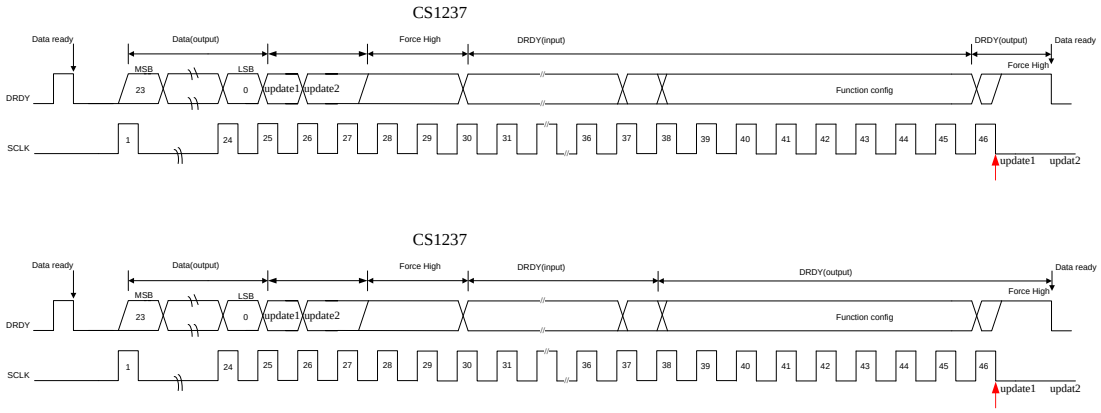
SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t4	$\overline{DRDY}/DOUT$ SCLK		0			ns
t5	SCLK		455			ns
t6	SCLK ( )		455			ns
t7	SCLK ( )		227.5		455	ns
t8				26.13		μs
t9	(1/data rate)	10Hz		100		ms
		40Hz		25		ms
		640Hz		1.5625		ms
		1280Hz		0.78125		ms

2.6.7

CS1237 SCLK $\overline{DRDY}/DOUT$



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$\overline{DRDY}/DOUT$

1. 1 24 SCLK ADC
2. 25 26 SCLK
3. 27 SCLK $\overline{DRDY}/DOUT$
4. 28 29 SCLK $\overline{DRDY}/DOUT$
5. 30 36 SCLK ( )
6. 37 SCLK $\overline{DRDY}/DOUT$ ($\overline{DRDY}/DOUT$ $\overline{DRDY}/DOUT$)
7. 38 45 SCLK (
   /)
8. 46 SCLK $\overline{DRDY}/DOUT$ $\overline{DRDY}/DOUT$
   update1/ update2

2.6.7.1 SPI

CS1237 2 7bits

10 CS1237

	0x65	Config
	0x56	Config

2.6.7.2 SPI

CS1237 Config

Config

	R/W		
			0x0C

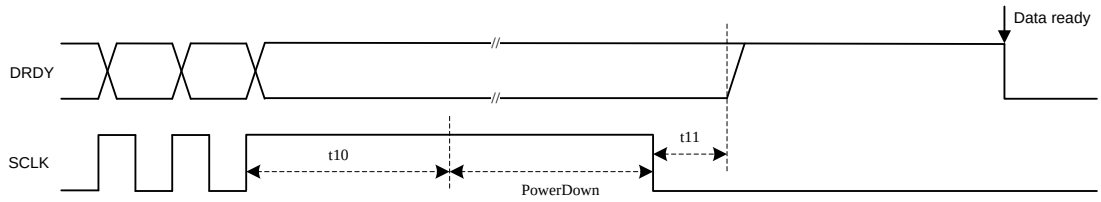
	B7	B6	B5	B4
		REF	ADC	
	B3	B2	B1	B0
	PGA			

11 Config

Bits		
[7]	-	**0 0 1**
[6]	REFO_OFF	**REF** REF 1= REF 0=REF
[5:4]	SPEED_SEL	**ADC** 10Hz SPEED_SEL[1:0] | 00 | ADC 10Hz 01 | ADC 40Hz 10 | ADC 640Hz 11 | ADC 1280Hz
[3:2]	PGA_SEL	**PGA** PGA 128 PGA_SEL=00 PGA_SEL[1:0] | 00 | 1 01 | 2 10 | 64 11 | 128
[1:0]	CH_SEL[1:0]	A CH_SEL[1:0] | 00 | A 01 | 10 | 11 |

2.6.8 Power down

SCLK 100μs CS1237 PowerDwon
0 SCLK



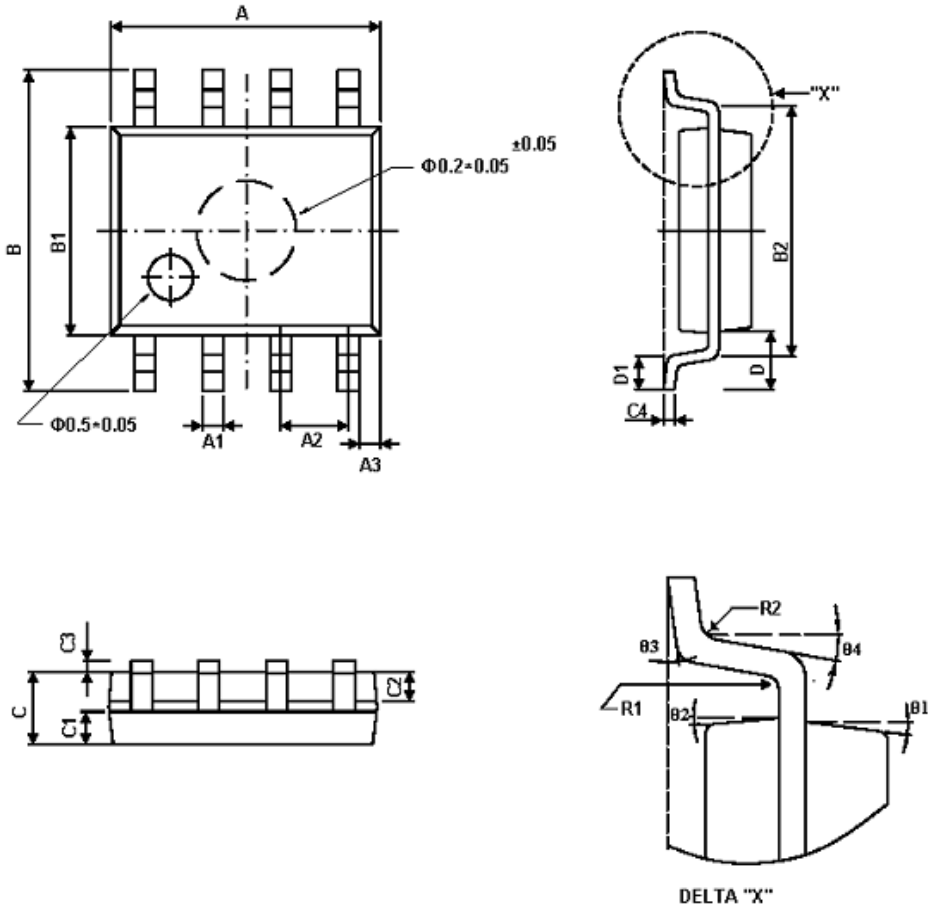
10 CS1237 PowerDown

symbol				
t10	SCLK	100μs		
t11	SCLK	10μs		

3

CS1237 SOP8

尺寸 / 标注	最小 （mm）	最大 （mm）	尺寸 / 标注	最小 （mm）	最大 （mm）
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	



11 SOP8